**CSC 364 – Computer Architecture**

Homework #3

1. A computer memory system is addressable by a 28 bit address bus. The cache in this system supports direct addressing, with a 4-bit word, and 19-bit line, and a 5-bit Tag. Answer the following questions:
   1. What is the size of this memory system?
   2. What is the size of cache in this system?
   3. How many words are in each cache line?
   4. What is the maximum number of different tags that can be loaded in this cache
2. Consider a machine with a byte addressable main memory of 216 bytes and a block size of 8 bytes. Assume that a direct cache consisting of 32 lines is used with this machine.
   1. How is the 16-bit memory address divided into Tag, Line number, and byte number
   2. Into what lines would bytes with each of the following addresses be stored:
      1. 0001 0001 0001 1011
      2. 1100 0011 0011 0100
      3. 1101 0000 0001 1101
      4. 1010 1010 1010 1010
   3. How many total bytes of memory can be stored in the cache?
3. For the hexadecimal main memory addresses 444444, 999999, CCCCCC, show the following information:
   1. Tag, Line, and Word values for a direct mapped cache using the format of (8-bit tag, 14-bit line and 2-bit word)
   2. For an associative-mapped cache, with a 22-bit tag, what are the tag and word values
4. Consider a CPU with the following specifications:

* It can access 256 words of memory, each word being 8 bits wide. The CPU does this by outputting a 8-bit address on its output pins A[7…0] and reading in the 8-bit value from memory on its inputs D[7…0]
* The CPU contains an 8-bit address register (AR), program counter (PC), accumulator (AC), data register (DR), and a 4-bit instruction register (IR).
* The CPU must realize the following instruction set. Note that β is an 8-bit value stored in the location immediately following the instruction

|  |  |  |
| --- | --- | --- |
| **Instruction** | **Instruction Code** | **Operation** |
| LD | 000XXXXX β | AC M[β] |
| STI | 001XXXXX β | β AC |
| ADD | 0100XXXX β | AC AC + M[β] |
| JUMP | 1000XXXX β | PC β |
| SKIP | 1100XXXX | PC PC + 1 |
| RST | 1110XXXX | PC 0, AC 0 |

Write and Design the following parts for this CPU:

1. RTL (Register Transfer language)
2. Data path / Register Section